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Integration of High-κ Dielectrics on Epitaxial (100), (110) and (111) Germanium for Multifunctional Devices

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With continued scaling of Si CMOS technology, new channel materials and device architectures are needed to address power consumption and constrained high-speed operation. With the demonstration of n-channel III-V transistors, the development of equivalent p-channel transistor is mandatory to realize energy-efficient CMOS logic. The bulk transport properties of Ge make it an ideal candidate for p-channel transistor. The ultra-high hole mobility Ge can be realized through a III-V/Ge/III-V transistor configuration with different surface orientations would enable much faster switching, thus addressing dynamic power consumption, while the superior high-κ gate dielectric and larger bandgap barrier would help minimize OFF-state leakage. This paper discusses the i) *in-situ* growth of III-V/Ge/III-V heterostructure, ii) tailor-made surface orientations of Ge enable to achieve both high-hole and high-electron mobilities, and iii) band offsets of high-κ dielectrics on crystallographic oriented epitaxial (100)Ge, (110)Ge, and (111)Ge layers using solid state molecular beam epitaxy.

Introduction

With continued transistor scaling, new channel materials and device architectures are needed for transistor miniaturization and to enhance transistor performance (1). According to the International Technology Roadmap for Semiconductors (2), new channel materials with superior transport properties in addition to metal gate/high-κ gate dielectric and multi-gate transistor configuration are required for further increase in transistor drive current and resultant ULSI performance improvement. One enticing approach is to replace the Si channel with high intrinsic hole mobility Ge for p-channel and low effective carrier mass III-V material for n-channel (3-11). Higher intrinsic carrier mobility of Ge will provide large drive current, and its smaller bandgap can enable operation at a lower voltages. In addition, high-κ dielectrics on Ge is essential to reduce the gate leakage current for low power operation. Thus, a combination of high-κ dielectric with high mobility Ge provides an opportunity for interface engineering and tailoring transistor performance. Alternative approaches are different surface orientations to improve carrier mobility (12-15), strain engineering (15-17) and optimal channel direction (18-22). The hole mobility of (110)Ge channel oriented along the <110> direction exhibited 2.3× higher hole mobility and 1.8× higher in electron mobility with (111)Ge compared with (100) and (110) orientations. However, the pre-defined channel thickness of high mobility material with different surface orientations that will enhance the transistor performances are extremely challenging. It has been demonstrated that the transistor fabricated on bulk (110)Ge exhibited hole mobility (μ_p) of 650cm^2/Vs (18) and higher electron mobility (μ_n) in bulk (111)Ge than bulk (100)Ge (23, 24). These crystallographic oriented epitaxial Ge layers on GaAs substrates and the detailed band offset properties of crystallographic oriented GaAs/Ge/GaAs heterostructures has been reported by Hudait *et al*. (25, 26). These advancements have intensified the research of Ge integration on Si using large bandgap buffer layer with the possibility of exceeding Moore's law. Moreover, low

bandgap Ge is compliant with the requirement of lower supply voltage operation of transistor and it is an excellent template for III-V heteroepitaxy and can be heterogeneously integrated on Si in conjunction with various optoelectronic components that could allow extending the Moore's law. However, there are many fundamental challenges that arise in attempting to use crystallographic oriented Ge as a p-channel or n-channel transistor namely: i) *common high-κ gate dielectric* on epitaxial (100)Ge, (110)Ge and (111)Ge layer with no interfacial layer, (ii) *breakthrough in Ge transistor configuration* using large bandgap buffers that will simultaneously provide higher ΔE_v and ΔE_c as well as remove parallel conduction from channel, iii) *challenge in making different surface orientations* of Ge for p-and n-channel transistor, and iv) *incorporation of strain* to achieve further boost in carrier mobility. Although, excellent device performances were achieved using high-κ gate dielectrics on bulk (100)Ge and oxide/(100)Ge band alignment properties; however, little attention has been devoted towards the integration of high-κ gate dielectrics on the epitaxial (100)Ge, (110)Ge and (111)Ge and its associated energy band alignment at each heterointerface. High-quality dielectric on these layers are essential to eliminate the formation of high density intrinsic defects, resulting in Fermi level unpinning at the oxide-semiconductor interface and the selected high-κ material should have valence and conduction band discontinuities (ΔE_v and ΔE_c) larger than 1eV relative to Ge to act as a barrier for both holes and electrons. *This paper will* presents a comprehensive study on the structural and band alignment properties of epitaxial GaAs/Ge/GaAs heterostructures as well as energy band alignment of atomic layer deposited Al_2O_3 and HfO_2 on (100)Ge, (110)Ge and (111)Ge substrates, grown by molecular beam epitaxy (MBE) and studied by x-ray photoelectron spectroscopy (XPS).

Growth of crystallographic oriented epitaxial (100), (110) and (111)Ge layers and their GaAs/Ge/GaAs heterostructures

The undoped epitaxial (100), (110) and (111)Ge layers and each oriented GaAs/Ge/GaAs heterostructures were grown using two separate MBE chambers for Ge and GaAs connected via ultra-high vacuum transfer chamber on crystallographic oriented (100)/6^o, (110) and (111)A GaAs substrates, respectively. Substrate oxide desorption was done at ~680°C for (100)/6^o-oriented GaAs, ~580°C for (110)-oriented GaAs and ~550°C for (111)A-oriented GaAs substrates under an arsenic overpressure of ~1x10^{-5} torr in a III-V MBE chamber. During the substrate oxide desorption, GaAs layer growth, and Ge layer after growth, reflection high energy electron diffraction (RHEED) patterns were recorded for each step of the growth process. An initial 0.2μm thick undoped GaAs buffer layer was then deposited on each GaAs substrate to generate a smooth surface prior to transferring each GaAs wafer to the Ge MBE chamber for Ge epilayer growth. The growth temperature was selected based on the surface terminated atoms of each GaAs substrate. The growth temperature of Ge was ~ 400^{o}C, it was selected in order to prevent the indiffusion of Ge into GaAs and outdiffusion of Ga and As into Ge film and the growth rate was ~0.1A/s, as determined by triple axis x-ray diffraction from Pendellösung thickness fringes as well as cross-sectional transmission electron microscopy. After the growth of Ge epitaxial layer and selected wafers were then transferred to III-V MBE chamber for subsequent GaAs layer growth. The surface reconstruction of each Ge layer was recorded by the RHEED system. Migration enhanced epitaxy with As_2 pre-layer was used for the subsequent GaAs growth on Ge epilayer.

The thickness of each epitaxial Ge layers was investigated ranged from about 75nm to 150nm. A 15keV electron beam energy at a glancing incident angle of 1^o to 4^o on the RHEED system was used to record the RHEED pattern during the growth in III-V MBE chamber. The epitaxy of undoped Ge and GaAs/Ge/GaAs double heterostructures were confirmed using a Panalytical MRD X'Pert Pro triple axis x-ray diffraction system with a CuKα1 line-focused x-ray source. The band alignment of each interface of *in-situ* grown GaAs/Ge/GaAs heterostructures was investigated using scanning XPS on a PHI Quantera SXM XPS system with a monochromated Al-Kα (energy of 1486.7eV) x-ray source, with a pass energy of 26eV and an exit angle of 45°. The GaAs and Ge epilayers were wet etched using $NH_4OH:H_2O_2:H_2O$

(2:1:200 volume ratio) for a required thickness of ~5-8nm and the surface oxide in each layer was removed prior to the XPS measurements. The different thicknesses of high-κ layers (Al_2O_3 and HfO_2) were deposited using atomic layer deposition (ALD) and epitaxial Ge layers were cleaned using $NH_4OH:H_2O_2:H_2O$ prior to high-κ deposition.

Results and discussion

X-ray rocking curves of GaAs/Ge/GaAs heterostructures

To determine the structural quality and relaxation state of Ge epitaxial film and the GaAs/Ge/GaAs double heterostructure grown on different crystallographic GaAs substrates, high-resolution triple axis x-ray (004) rocking curves were recorded. Fig. 1 shows a rocking curve from the (004) Bragg lines of GaAs/Ge/GaAs double heterostructure grown on (100)/6°, (110) and (111)A GaAs substrates, where the epitaxial Ge layer thickness is significantly lower than the critical layer thickness. The appearance of Pendellösung oscillation fringes on both sides of Ge and GaAs peaks implies a parallel and very sharp heterointerface presents in this structure. This interference originates from the beating of two x-ray wave fields inside of a crystal. One of the wave fields is generated at the interface between the GaAs and Ge as well as another wave field on the surface of the Ge layer. As a result, interference can only be observed in crystals that have almost perfectly parallel boundaries (27). The degree of relaxation of each Ge layer was limited to only 5% in each case. The minimal relaxation and the thickness fringes observed here that the quality of the GaAs/Ge/GaAs heterostructure on (100), (110) or (111)A GaAs substrates are high-quality.

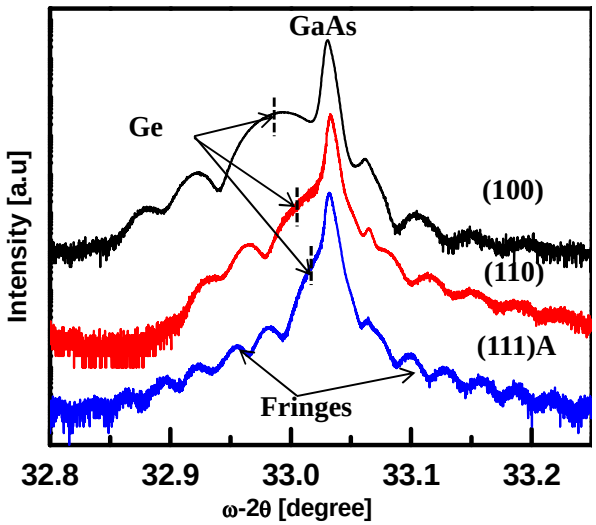

Fig. 1: X-ray rocking curves from the (004) reflection of (a) 53nm GaAs/150nm Ge/GaAs heterostructure on (100)/6° GaAs, (b) 112nm Ge on (110)GaAs, and (c) 140nm Ge on (111)A GaAs substrate, respectively. The Pendellösung oscillations in the rocking curve confirm the high crystalline quality of the Ge epitaxial layer.

Band alignment properties of GaAs/Ge/GaAs heterostructures

A great deal of attention has been devoted to the determination of ΔE_v of Ge on GaAs heterojunction; however, minimal work has been done on the determination of band offset of GaAs on epitaxial Ge grown on different crystallographic GaAs substrates. It was believed due to the more challenging polar-on-nonpolar epitaxy of GaAs on Ge heterojunction. Conduction band offsets varying from 0.09 to 0.54eV can be found in the literature, a range corresponding to 68% of the energy gap of Ge (29). The reason is partly due to measurement errors and polar-on-nonpolar growth (28). As we know that the two semiconductors having different bandgap results in band discontinuities when in contact and these band discontinuities play a crucial role in the electrical transport properties of a heterojunction devices like quantum well field effect transistors (FETs), heterojunction bipolar transistors, tunnel FETs, III-V multijunction solar cells, superlattice photodetectors, heterostructure lasers, etc. The transport properties of all these heterojunction based devices strongly depend on (i) band discontinuities, (ii) interface states, and (iii) potential-barrier height. Fig. 2 shows the histogram of ΔE_V distribution obtained from GaAs/Ge/GaAs double heterostructures (26). One can find that the substrate orientation has a strong

influence on the band offset properties, which is believed to be the quality of the heterojunction growth, the surface reconstruction and charge neutrality at each heterointerface. Several models have been developed (29) to explain the difference in band offset values. Fang and Howard (30) and Grant *et al.* (31, 32) have carried out the valence band offset of Ge on different oriented GaAs substrates and demonstrated a relationship of $\Delta E_V(111)Ga < \Delta E_V(\bar{1}\bar{1}\bar{1})As < \Delta E_V(110)$ and $\Delta E_V(111)Ga < \Delta E_V(100)Ga < \Delta E_V(110) < \Delta E_V(100)As < \Delta E_V(\bar{1}\bar{1}\bar{1})As$ using capacitance-voltage and XPS method, respectively. Although, the magnitude of variation of ΔE_v they have observed is consistent in some orientations, our results contradict the ΔE_v relation above and achieved a valence band offset relation of $\Delta E_V(111)Ga > \Delta E_V(110) > \Delta E_V(100)As$ after careful investigation of XPS results. Furthermore, this ΔE_v relation holds good for the growth of GaAs on Ge which was grown on (100), (110) and (111)A GaAs substrates. The highest ΔE_V value for both upper and bottom interface of GaAs/Ge/GaAs was obtained on (111)A GaAs substrate. Thus, comparison of band offset between experiment and theory are undoubtedly exciting and our *in-situ* grown GaAs/Ge/GaAs heterostructures with crystallographic orientations provide a promising path for both p-and n-channel transistor applications. To prevent the carrier spill-off to the upper barrier layer due to the lower ΔE_v at the upper GaAs/Ge interface compared to Ge/GaAs bottom interface, composite gate dielectric consists of GaAs and high-*k* layer (e.g., Al_2O_3, HfO_2) on upper GaAs would enable high-performance multifunctional devices

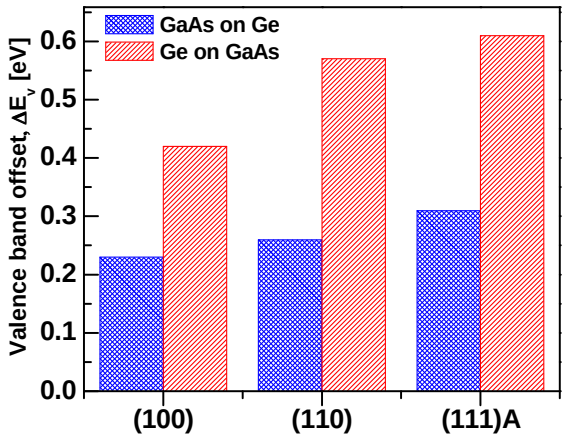

Fig. 2: Histogram of valence band offset distribution obtained from GaAs/Ge/GaAs heterostructures.

TEM micrograph of HfO_2/(110)Ge heterojunction

Fig. 3 shows a high-resolution cross-sectional transmission electron microscopy (TEM) micrograph of HfO_2/(110)Ge interface. This TEM micrograph shows a sharp HfO_2/(110)Ge interface. The HfO_2 thickness measured by TEM is ~5nm, consistent with the ALD deposited thickness. From this figure, one can find that there is no interfacial layer formed during the deposition of HfO_2 on (110)Ge layer which implies that the removal of interfacial oxide can be easily obtained on (110)Ge and thus have a potential advantage of HfO_2/(110)Ge for high-hole mobility p-channel transistor application (33). On contrary, a thinner interfacial layer consisting of a mixture of GeO and GeO_2, as reported by several researchers (34), on (100)Ge layer (35). On one hand, removal of this unwanted layer is essential due to the lower dielectric constant of GeO_2 as well as poor chemical and thermal stability (34). Further, the

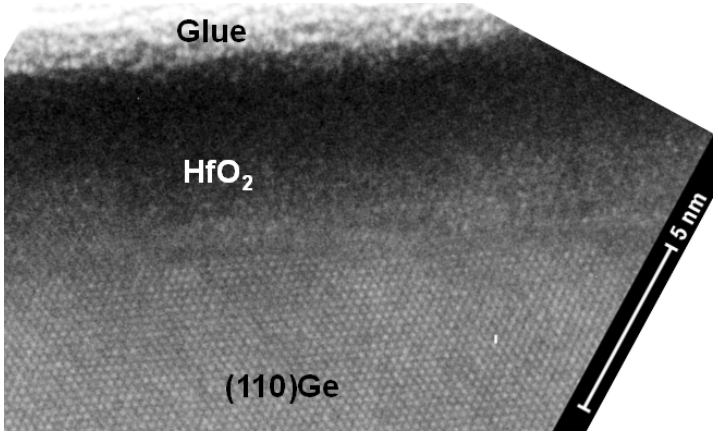

Fig. 3: Cross-sectional TEM micrograph of HfO_2/(110)Ge heterointerface.

elimination of this poor quality oxide layer is desired to obtain better electrical transport characteristics namely, equivalent oxide layer thickness, interface states, capacitance-voltage hysteresis, and frequency dispersion. The relatively unstable nature of Ge oxide implies that the removal of unwanted interfacial oxide can be easily achieved and thus have a potential advantage of high-κ on Ge system (34).

Band alignment properties of Al_2O_3/Ge and HfO_2/Ge heterostructures

The valence band offset, ΔE_v of 3.3±0.1eV between the Al_2O_3 and the (100)Ge has been studied by several researchers using different deposition methods of Al_2O_3 (36). However, the experimental band offset values on the (110)Ge and (111)Ge epitaxial layers would provide a better insight into the electrical transport properties of the MOS capacitors for p-channel and n-channel MOSFET applications. Therefore, the energy band alignment at the high-κ and crystallographic Ge interface is of great importance, since the sufficient barriers for electron and hole are needed to suppress the tunneling leakage current. Also, the reported hole mobility is higher on (110)Ge and electron mobility on (111)Ge, thus, the measured ΔE_v and ΔE_c values of Al_2O_3 relative to (110)Ge and (111)Ge will provide further insights into the predicted electrical transport mechanisms in the predefined Ge channel layer thickness grown on a large bandgap GaAs barrier layer. Fig. 4 shows the histogram of ΔE_v and ΔE_c distribution obtained from ALD Al_2O_3 oxide film on epitaxial crystallographic oriented Ge layers (37). One can find that the crystallographic orientation of Ge epilayer has a strong influence on the band offset properties, which is believed to be the quality of the Ge/GaAs heterojunction growth, the surface reconstruction of Ge and the interface quality at the Al_2O_3/Ge heterointerface. From this result, one can find that the ΔE_v and ΔE_c of Al_2O_3 on crystallographic oriented Ge epilayers are well above 1eV, as needed for blocking electrons and holes (38) for carrier transport in the fabricated Ge MOSFETs.

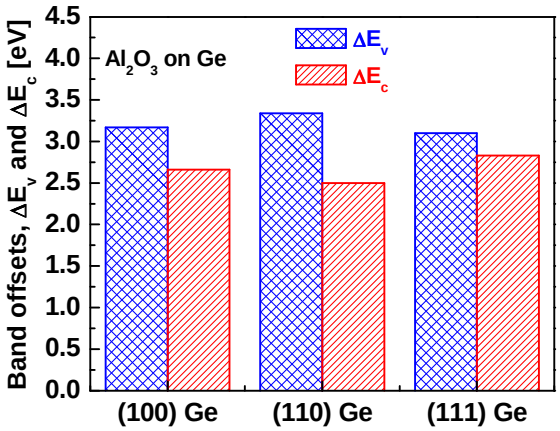

Fig. 4: Histogram of band offset distribution obtained from Al_2O_3/Ge heterointerface on crystallographic oriented Ge layers.

The ΔE_v of 2.8±0.1eV between the HfO_2 and the (100)Ge was studied by several researchers using different deposition methods of HfO_2 (39). Conduction band offset, ΔE_c varying from 2.0 to 2.2eV was found and the reason was partly due to the measurement errors associated with the bandgap of HfO_2 layer. However, the experimental band offset values on the (110)Ge and (111)Ge epitaxial layers would provide better understanding into the electrical transport properties of the p-channel and n-channel MOSFET, respectively. Fig. 5 shows the histogram of ΔE_v and ΔE_c distribution obtained from atomic layer HfO_2 oxide film deposited on crystallographically oriented Ge layers (40). One can find from this figure that the measured valence and conduction band

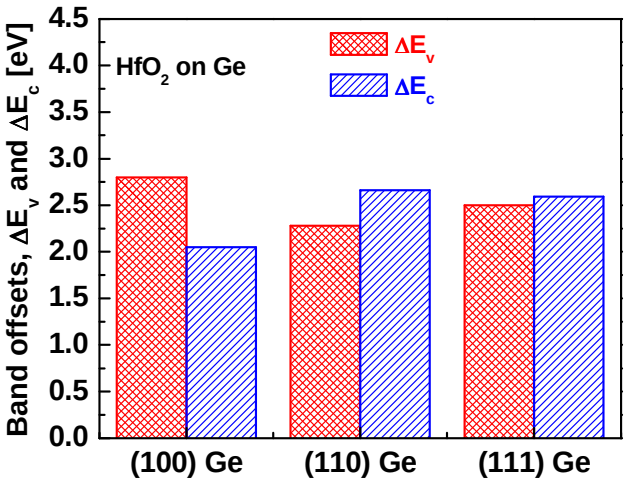

Fig. 5: Histogram of band offset distribution obtained from HfO_2/Ge heterointerface on crystallographically oriented epitaxial Ge layers

offsets were above 2eV, required for confining carriers inside the Ge channel to reduce the leakage current. These band discontinuities play a central role on the electrical transport properties of MOSFET devices, since sufficient band offset barriers were needed to suppress the tunneling leakage current for both electrons and holes. *In both Al_2O_3 and HfO_2, band offsets were larger than 1eV, needed for carrier leakage.* Thus, these band alignment properties offer a potential advantage for designing p-and n-channel Ge metal-oxide semiconductor field effect transistors.

Conclusions

In conclusion, we have shown that high-quality epitaxial GaAs/Ge/GaAs heterostructures can be grown *in-situ* on (100), (110) and (111)A GaAs substrates using two separate MBE chambers, confirmed by x-ray diffraction. Using XPS data, variations in band discontinuities related to the crystallographic orientation is $\Delta E_V(111)Ga > \Delta E_V(110) > \Delta E_V(100)As$. Cross-sectional TEM micrograph shows a sharp HfO_2/(110)Ge heterointerface. Valence band offsets of 3.17eV, 3.34eV, and 3.10eV have been derived from XPS data on Al_2O_3/(100)Ge, Al_2O_3/(110)Ge, Al_2O_3/(111)Ge heterointerfaces, respectively. Moreover, valence band offsets of 2.8eV, 2.28eV, and 2.5eV were measured from HfO_2/(100)Ge, HfO_2/(110)Ge, HfO_2/(111)Ge heterointerfaces, respectively. The high-quality heterointerface and the band offset parameters for carrier confinement can offer a promising virtual substrate technology integrated on Si substrate for extending the performance and application of Ge-based p-and n-channel metal-oxide field effect transistor design and multifunctional devices.

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